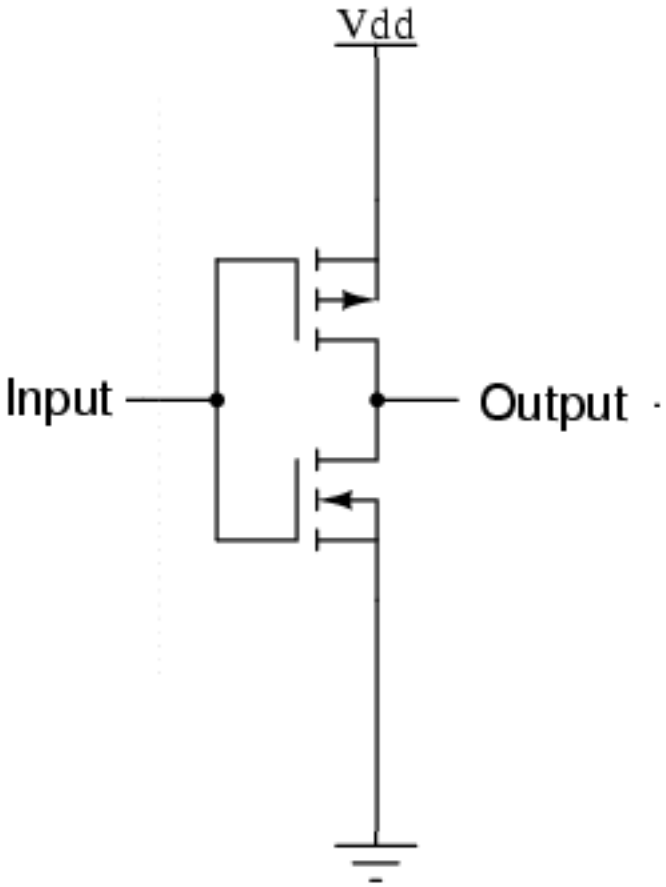
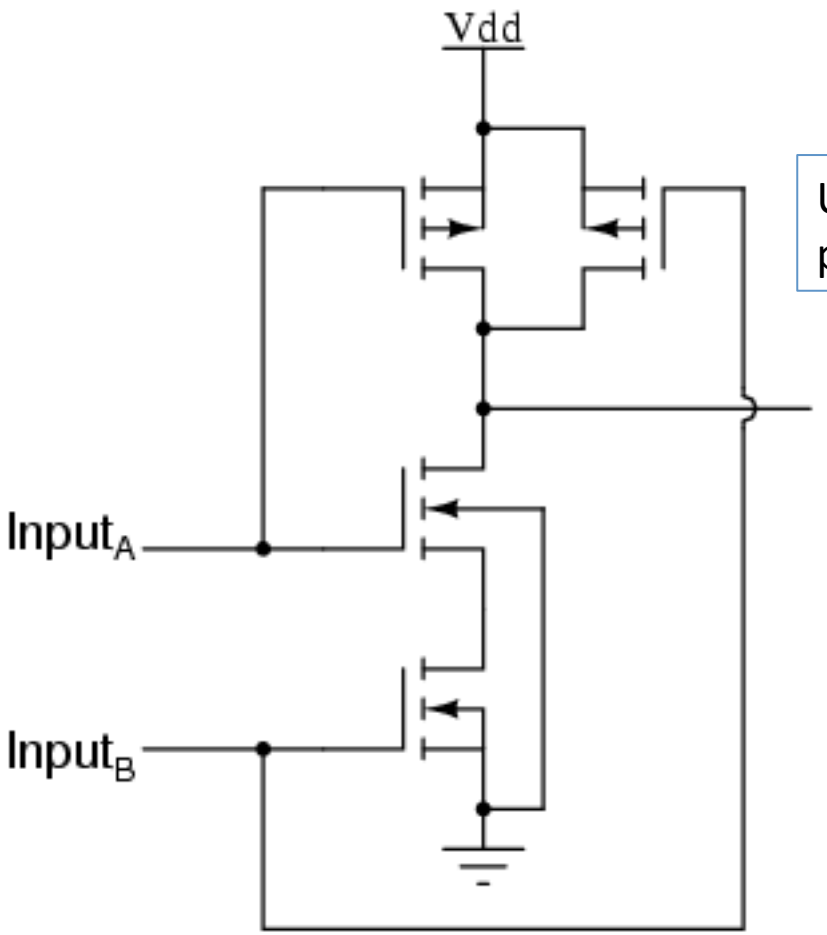
NOT CMOS



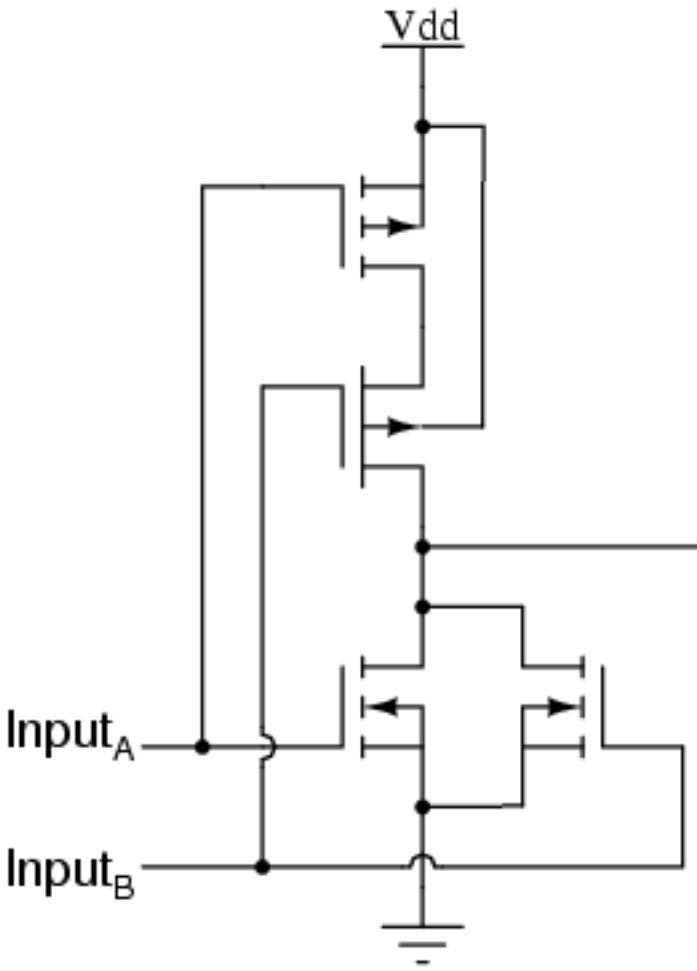
NAND CMOS



Un gate in parallelo per ogni input

Un gate in serie per ogni input

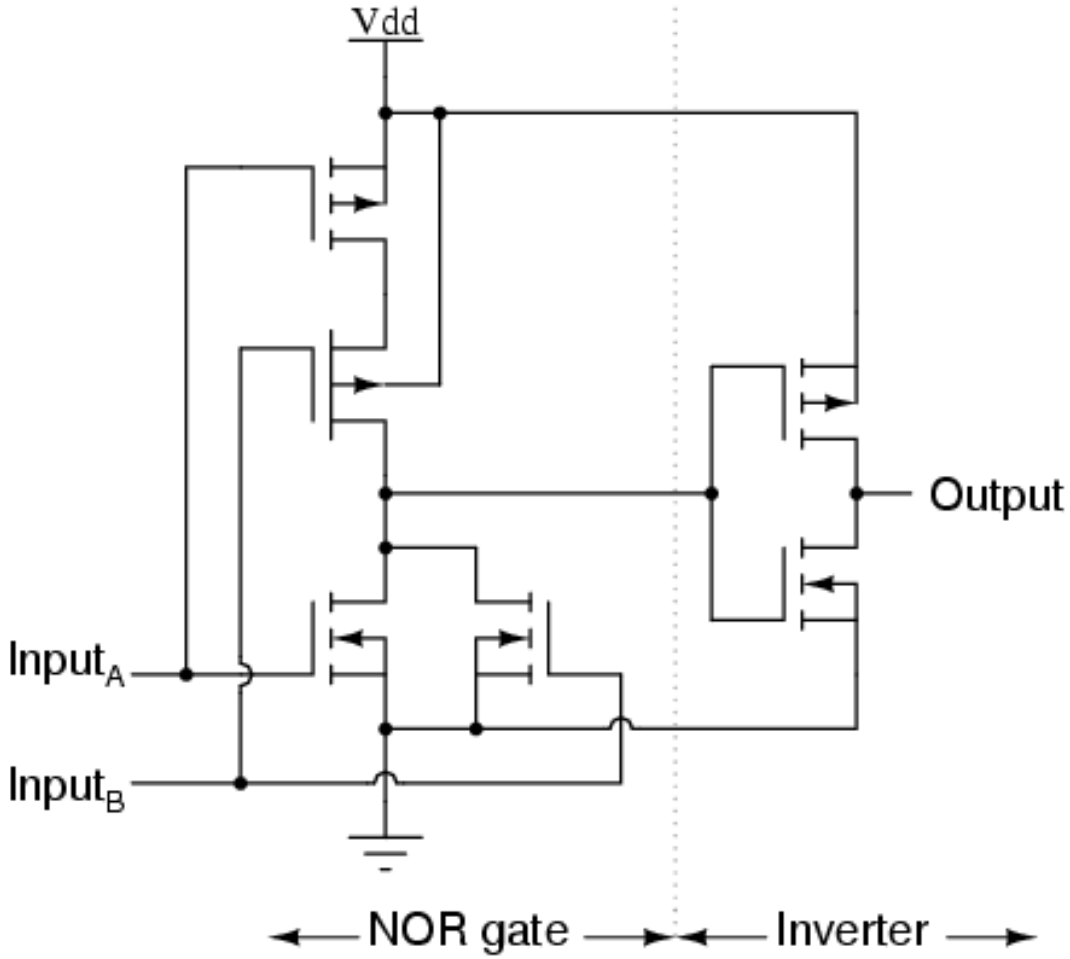
NOR CMOS



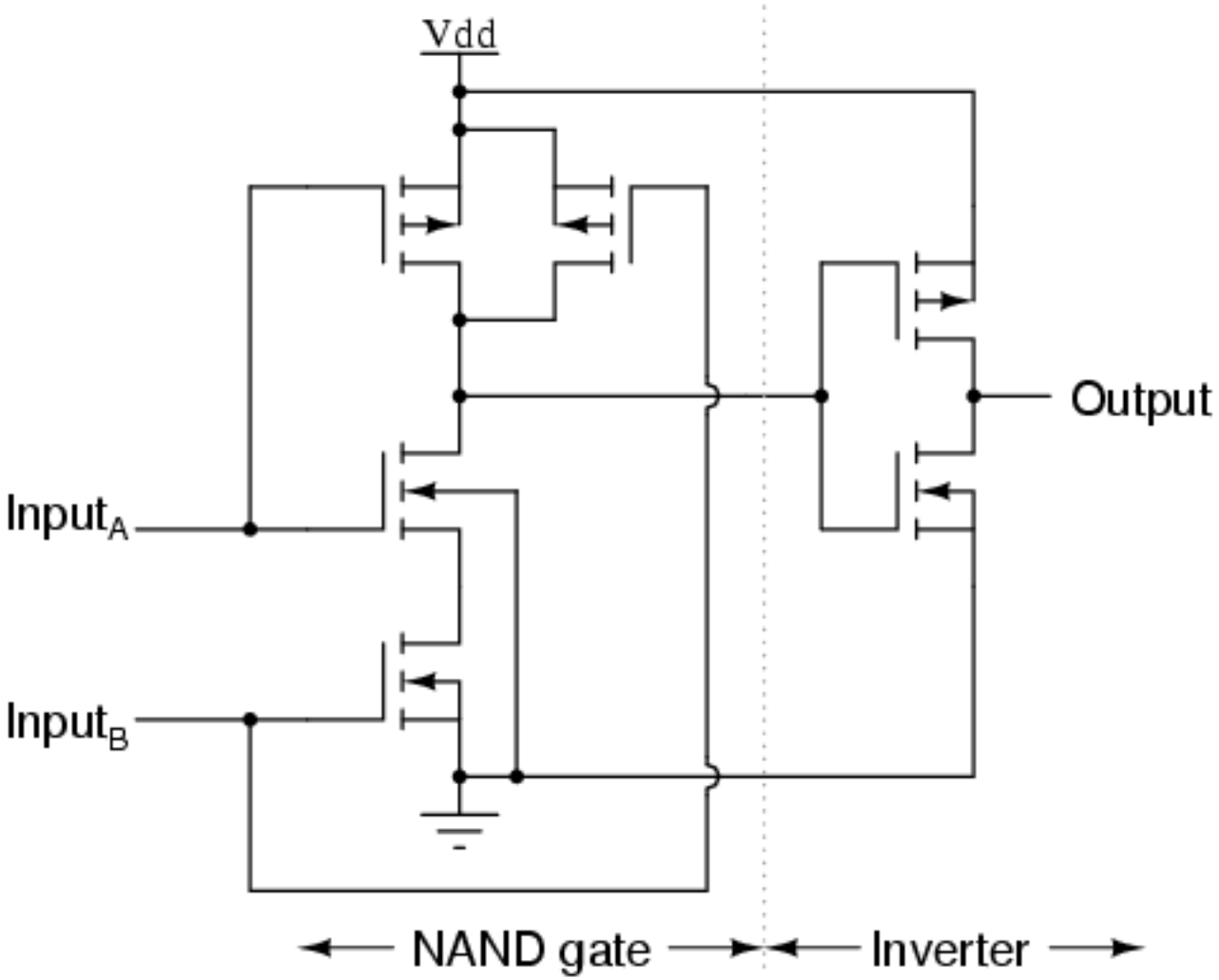
Un gate in serie per ogni input

Un gate in parallelo per ogni input

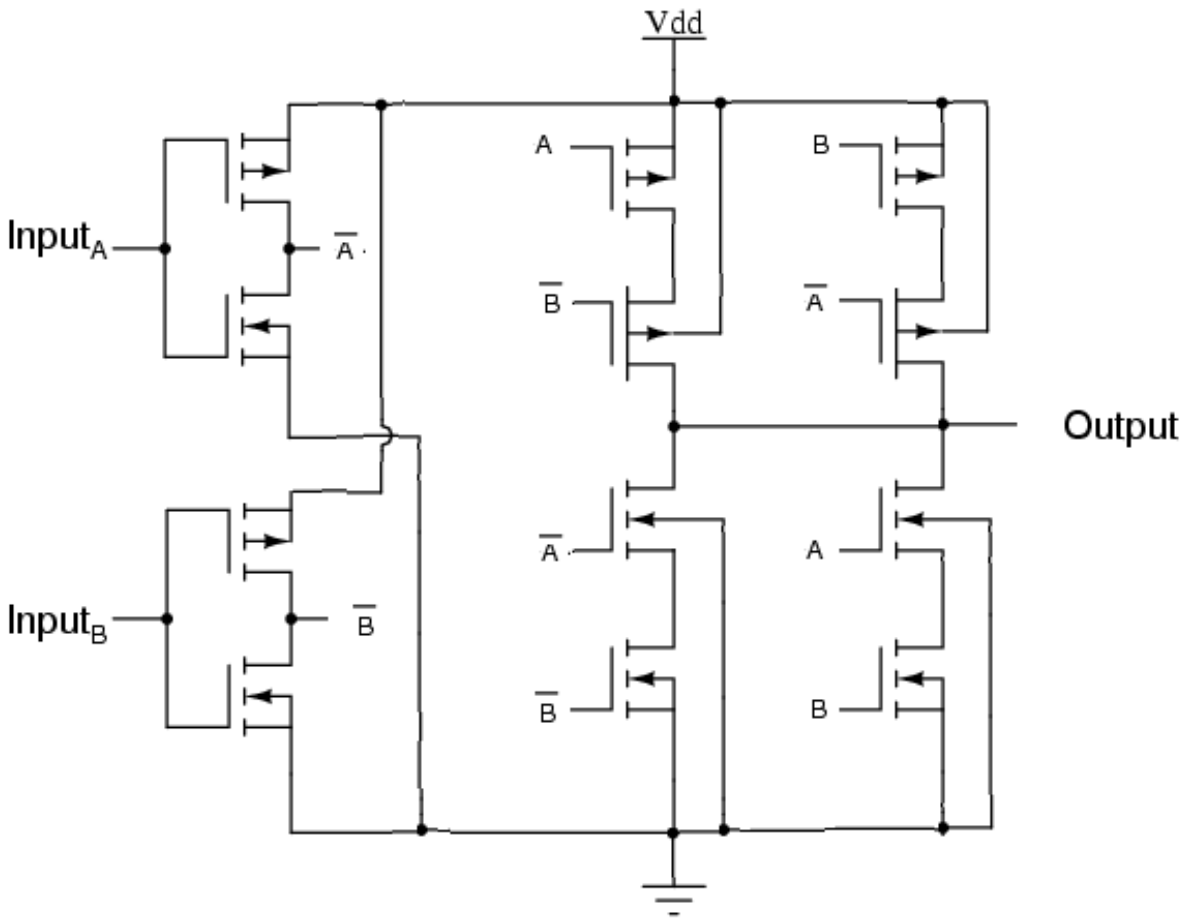
OR CMOS



AND CMOS



XOR CMOS


Vdd
Input$_A$
Input$_B$
$\overline{A}$
$\overline{B}$
A
B
$\overline{A}$
$\overline{B}$
A
B
Output

XNOR CMOS